What is claimed is:

1. A semiconductor display device comprising:

a source signal line drive circuit unit constituted by plural thin-film transistors;

a gate signal line drive circuit unit constituted by plural thin-film transistors; and

a pixel unit in which plural pixel thin-film transistors are arranged like a matrix; wherein,

the gate signal line drive circuit has at least one tristate buffer per a gate signal line;

the tristate buffer has:

a first circuit that includes a pair of n-channel thin-film transistor and p-channel thin-film transistor; and

a second circuit that includes a pair of n-channel thin-film transistor and p-channel thin-film transistor;

the source region of the n-channel thin-film transistor in the first circuit is electrically connected, at a first connection point, to the source region of the p-channel thin-film transistor of the second circuit;

a first power source is electrically connected to the source region of the p-channel thin-film transistor of the first circuit;

a second power source having a potential lower than that of the first power source is electrically connected to the first connection point;

a third power source having a potential lower than the second power source is electrically connected to the source region of the n-channel thin-film transistor of the second circuit; and

an output signal line of the first circuit and an output signal line of the second circuit are both electrically connected to the gate signal line at a second connection point.

2. A semiconductor display device comprising:

a source signal line drive circuit unit constituted by plural thin-film transistors;

a gate signal line drive circuit unit constituted by plural thin-film transistors; and

a pixel unit in which plural pixel thin-film transistors are arranged like a matrix; wherein,

the gate signal line drive circuit has at least one tristate buffer per a gate signal line;

the tristate buffer has:

a first circuit that includes a pair of n-channel thin-film transistor and p-channel thin-film transistor; and

a second circuit that includes a pair of n-channel thin-film transistor and p-channel thin-film transistor;

the source region of the n-channel thin-film transistor in the first circuit is electrically connected, at a first connection point, to the source region of the p-channel thin-film transistor of the second circuit;

a first power source is electrically connected to the source region of the p-channel thin-film transistor of the first circuit;

a second power source having a potential lower than that of the first power source is electrically connected to the first connection point;

a third power source having a potential lower than the second power source is electrically connected to the source region of the n-channel thin-film transistor of the second circuit;

an output signal line of the first circuit and an output signal line of the second circuit are both electrically connected to the gate signal line at a second connection point;

a gate signal line selection pulse is input to the gate of the p-channel thin-film transistor of the first circuit;

a first signal is input to the gate of the n-channel thin-film transistor of the first circuit;

a second signal is input to the gate of the p-channel thin-film transistor of the second circuit;

a third signal is input to the gate of the n-channel thin-film transistor of the second circuit;

when a frame period in which the opposing electrode assumes a high potential is regarded to be a first frame period and a frame in which the opposing electrode has a low potential is regarded to be a second frame period during the opposing common inverse drive, the third signal is input during a fly-back period of when the first frame period is being changed over to the second frame period;

the second signal is input just before the gate signal line selection pulse is input; and

the first signal is input during a period of from when the gate signal line selection pulse is output in the second frame period until when the second signal is output in the first frame period, and during a period of from when the gate signal line selection pulse is output in the first frame period until when the third signal is input in the fly-back period.

3. A semiconductor display device according to claim 1 or 2, wherein the first signal is obtained by directly inputting a signal from an external unit.

4. A semiconductor display device according to claim 1 or 2, wherein the first signal is the one output from a logic circuit that receives the gate signal line selection pulse and the third signal.

5. A semiconductor display device according to claim 1 or 2, wherein the first signal is the one output from a logic circuit that receives any one of the signals or plural signals fed to the gate signal line drive circuit from an external unit.

6. A semiconductor display device according to claim 1 or 2, wherein the first signal is the one output from a NOR circuit by inputting the gate signal line

selection pulse and the third signal to a reset/set flip-flop circuit and, then, by inputting the output of the reset/set flip-flop circuit and the gate signal line selection pulse to the NOR circuit.

7. A semiconductor display device according to claim 1 or 2, wherein the second signal is obtained by directly inputting a signal from an external unit.

8. A semiconductor display device according to claim 1 or 2, wherein the second signal is a gate signal line selection pulse output to a stage preceding the gate signal line selection pulse.

9. A semiconductor display device according to claim 1 or 2, wherein the third signal is obtained by directly inputting a signal from an external unit.

10. A semiconductor display device comprising:

a source signal line drive circuit unit constituted by plural thin-film transistors;

a gate signal line drive circuit unit constituted by plural thin-film transistors; and

a pixel unit in which plural pixel thin-film transistors are arranged like a matrix; wherein,

the gate signal line drive circuit has at least one tristate buffer per a gate signal line;

the tristate buffer has:

a first circuit that includes a pair of n-channel thin-film transistor and p-channel thin-film transistor;

a second circuit that includes a pair of n-channel thin-film transistor and p-channel thin-film transistor;

a reset/set flip-flop circuit; and

a NOR circuit;

the source region of the n-channel thin-film transistor in the first circuit is electrically connected, at a first connection point, to the source region of the p-channel thin-film transistor of the second circuit;

a first power source is electrically connected to the source region of the p-channel thin-film transistor of the first circuit;

a second power source having a potential lower than that of the first power source is electrically connected to the first connection point;

a third power source having a potential lower than the second power source is electrically connected to the source region of the n-channel thin-film transistor of the second circuit;

an output signal line of the first circuit and an output signal line of the second circuit are both electrically connected to the gate signal line at a second connection point;

a gate signal line selection pulse is input to the gate of the p-channel thin-film transistor of the first circuit;

a first signal is input to the gate of the n-channel thin-film transistor of the first circuit;

a second signal is input to the gate of the p-channel thin-film transistor of the second circuit;

a third signal is input to the gate of the n-channel thin-film transistor of the second circuit;

when a frame period in which the opposing electrode assumes a high potential is regarded to be a first frame period and a frame in which the opposing electrode has a low potential is regarded to be a second frame period during the opposing common inverse drive, the third signal is input during a fly-back period of when the first frame period is being changed over to the second frame period;

the second signal is input just before the gate signal line selection pulse is input; and

the first signal is an output signal of a NOR circuit that receives the gate signal line selection pulse and a set output signal obtained by inputting a gate

signal line selection pulse to the reset signal input line of the reset/set flip-flop circuit and by inputting the third signal to the set signal input line..

11. A semiconductor display device according to claim 10, wherein the second signal is obtained by directly inputting a signal from an external unit.

12. A semiconductor display device according to claim 10, wherein the second signal is a gate signal line selection pulse output to a stage preceding the gate signal line selection pulse.

13. A semiconductor display device according to claim 10, wherein the third signal is obtained by directly inputting a signal from an external unit.

14. A semiconductor display device according to claim 1, wherein said semiconductor display device is incorporated into an electronic device selected from the group consisting of a cellular phone, a video camera, a mobile computer, a head-mount display, a television, a portable book, a personal computer, a digital camera, and a DVD player.

15. A semiconductor display device according to claim 2, wherein said semiconductor display device is incorporated into an electronic device selected from the group consisting of a cellular phone, a video camera, a mobile computer, a head-mount display, a television, a portable book, a personal computer, a digital camera, and a DVD player.

16. A semiconductor display device according to claim 10, wherein said semiconductor display device is incorporated into an electronic device selected from the group consisting of a cellular phone, a video camera, a mobile computer, a head-mount display, a television, a portable book, a personal computer, a digital camera, and a DVD player.

17. A semiconductor display device comprising:

a source signal line drive circuit unit and a gate signal line drive circuit unit formed over a substrate, said gate signal line drive circuit having at least one tristate buffer per a gate signal line;

said tristate buffer comprising:

at least a first circuit and a second circuit,

a first power source electrically connected to said first circuit;

a second power source having a potential lower than that of said first power source; and

and a third power source having a potential lower than that of said second power source and electrically connected to said second circuit.

18. A semiconductor display device according to claim 17, wherein said semiconductor display device is incorporated into an electronic device selected from the group consisting of a cellular phone, a video camera, a mobile computer, a head-mount display, a television, a portable book, a personal computer, a digital camera, and a DVD player.

19. A method of driving a semiconductor display device having a source signal line drive circuit unit constituted by plural thin-film transistors, a gate signal line drive circuit unit constituted by plural thin-film transistors, and a pixel unit in which plural pixel thin-film transistors are arranged like a matrix, said method comprises:

wherein pixel TFTs constituting an active matrix circuit are driven by using three kinds of potentials which are a first power-source potential, a second power-source potential and a third power-source potential.

20. A method according to claim 19, wherein said semiconductor display device is incorporated into an electronic device selected from the group consisting of a cellular phone, a video camera, a mobile computer, a head-mount display, a

television, a portable book, a personal computer, a digital camera, and a DVD player.